Description

EEPROM WITH SOURCE LINE VOLTAGE STABILIZATION MECHANISM

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation in part of commonly owned, U.S. Patent Application Ser. No. 10/065,591, "BI-DIRECTIONAL FOWLER-NORDHEIM TUNNELING FLASH MEMORY", by Ching-Sung Yang, Shih-Jye Shen, and Ching-Hsiang Hsu, filed October 31, 2002.

BACKGROUND OF INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a nonvolatile semiconductor memory, and more particularly, to a bi-directional Fowler-Nordheim (FN) write/erase flash memory utilizing a compatible and low-electric consumption operation mode. An induced capacitor is created between a cell N well and an underlying deep P well to help stabilize source line voltage during read operations. According to the

present invention, high-speed code flash memory and high-density data flash memory can be integrated on a single chip.

[0004] 2. Description of the Prior Art

[0005] Recently, flash electrically erasable programmable read-only memories (EEPROMs) have gained substantial interest as the best solution for electrically rewritable nonvolatile data storage. These semiconductor memories, which have been broadly used on digital products such as digital cameras, cell phones, video game apparatuses, personal digital assistants (PDA), and so on, combine the high integration density and the high programming speed of EPROMs with the higher functionality of EEPROMs by offering electrical in-circuit erasability. In general, flash memories are categorized into NOR cell and NAND cell types. As known in the art, NOR type flash memory can be operated at higher read speeds and is thus suited for code flash, which primarily implements program transformation. NAND type flash memory has a relatively low read speed but higher density so that it is typically used as data flash, which primarily implements data access or data storage.

[0006] Please refer to Fig.1. Fig.1 is a cross-sectional view illus-

trating a conventional NAND type EEPROM 10. As shown in Fig.1, the NAND type EEPROM 10 comprises an N-type semiconductor substrate 12, a P-type semiconductor well 14 located in the semiconductor substrate 12, a plurality of NAND cell blocks (B_1, $B_2 \sim B_N$) in one column located on the P-type semiconductor well 14, and a local bit line BL1 located over the column of NAND cell blocks (B_1, $B_2 \sim B_N$). The prior art NAND type EEPROM 10 further comprises another column of NAND cell blocks (not shown) next to the column of NAND cell blocks (B_1, $B_2 \sim B_N$) of Fig.1, and both columns of NAND cell blocks are formed on the same (commonly used) P-type semiconductor well 14 having a well depth that is deeper than the depth of STI regions. Each of the NAND cell blocks (B_1, $B_2 \sim B_N$) comprises a plurality of rewritable NMOS memory transistors ($M_0 \sim M_n$) connected in series along a direction of the local bit line BL1. The rewritable NMOS memory transistors ($M_0 \sim M_n$) are a stacked gate structure, as known in the art, each having an upper control gate 20 and a lower floating gate 22 for storing charges. Rows of word lines are connected to the control gates 20 of memory transistors ($M_0 \sim M_n$). At two opposite ends of each of the NAND cell blocks (B_1, $B_2 \sim B_N$) are provided a bit line selection transis-

tor SGB and a source line selection transistor SGS, respectively, where one terminal of the bit line selection transistor SGB is electrically connected to the local bit line BL1, and one terminal of the source line selection transistor SGS is electrically connected to a source line SL.

[0007] However, the above-mentioned flash memory architecture has a drawback in that it consumes a great deal of electricity during a data program operation, leading to a decreased duration of batteries used in digital products. When implementing a data program operation regarding the prior art NAND type EEPROM 10, by way of example, a high voltage such as 20V is applied on a selected word line, and a high voltage such as 12V is applied to unselected word lines to conduct N channels thereof. Consequently, the prior art NAND type EEPROM 10 has very high power consumption. Furthermore, since high voltages, for example, 20V (for the selected cell) and 12V (for non-selected cells), are required to be applied on the selected and un-selected word lines, the programming speed is decelerated, and corresponding reliability problems such as junction breakdown or over-erase will occur. Moreover, since the operation mode of the prior art NAND flash is different from the operation mode of conventional NOR

flash, it is difficult to integrate both types of memories onto a single chip. This is because NAND-type data flash memory utilizes a Fowler-Nordheim (FN) tunneling mechanism to implement data programming, while the NOR-type code flash utilizes a hot-carrier injection mechanism to implement data programming. In addition, the prior art flash memory occupies more chip area, thus more costly.

SUMMARY OF INVENTION

[0008] Accordingly, it is the primary objective of the claimed invention to provide a low-energy consumption nonvolatile memory, which is operated at relatively low voltages, thereby prolonging duration of batteries of portable electric apparatuses.

[0009] It is another objective of the claimed invention to provide an electrically erasable programmable read-only memory (EEPROM) that occupies smaller chip area and can be operated by using a reliable operation mode without the fear of over-erasing.

[0010] It is still another objective of the claimed invention to provide an EEPROM capable of integrating high-density NAND flash memory and low-density/high-speed NOR flash memory on a single chip.

[0011] It is still another objective of the claimed invention to pro-

vide an EEPROM comprising a unique isolated buried local bit line and capable of implementing bi-directional FN write/erase operations.

[0012] It is yet another objective of the claimed invention to provide an integrated single chip combining BiAND-type EEPROM with 2T-BiNOR EEPROM and having compatible operation (erase/write/read) modes.

[0013] In accordance with the above objectives, the claimed invention is addressed to a specific low-voltage nonvolatile memory array comprising: a substrate, a cell well of a first conductivity type formed in the substrate, and columns of buried bit lines of a second conductivity type formed within the cell well. The columns of the buried bit lines are isolated from each other and each of which is further divided into plurality of sub-bit line segments with deeply doped source wells of the first conductivity type connected to the cell well. A plurality of memory cell blocks are serially arranged over one of the columns of buried bit lines, wherein a memory cell block corresponds to a sub-bit line segment, and each of the memory cell blocks comprises at least one memory transistor having a stacked gate, a source, and a drain. A local bit line overlies the memory cell blocks and is electrically connected

to the drain of the memory transistor via a contact plug short-circuiting the drain and the subjacent buried bit line thereof.

[0014] In accordance with one feature of the claimed invention, a nonvolatile memory device comprises: a substrate, a cell well of a first conductivity type formed in the substrate, columns of buried bit lines of second conductivity type formed within the cell well. The columns of the buried bit lines are isolated from each other and each of which is further divided into plurality of sub-bit line segments with deeply doped source wells of the first conductivity type connected to the cell well of first conductivity type. A plurality of memory cell blocks are serially arranged over one of the columns of buried bit lines, wherein a memory cell block corresponds to a sub-bit line segment, and each of the memory cell blocks comprises at least one memory transistor having a control gate, a floating gate, a source, and a drain. The nonvolatile memory device of this invention further comprises rows of word lines, each of which connects to the control gate of one of the memory transistors. A local bit line overlies the memory cell blocks and electrically connected to the drain of the memory transistor via a contact plug short-circuiting the drain and

the subjacent buried bit line. The nonvolatile memory device of this invention further comprises columns of main bit lines. The columns of the buried bit lines are isolated from each other with shallow trench isolations.

[0015] According to one preferred embodiment of the claimed invention, the deeply doped source well of first conductivity type serves as the source of the memory transistor. The source line is electrically coupled to the cell N well to avoid large read current bounce or potential power crash during read operations. According to another preferred embodiment of the claimed invention, the memory cell block further comprises a selection transistor having one end serially connected to the source of the memory transistor and the deeply doped source well serves as a source of the selection transistor. According to yet another embodiment of the claimed invention, each of the memory cell blocks comprises a plurality of memory transistors serially connected to each other to form a NAND memory cell array.

[0016] Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0018] Fig.1 is a cross-sectional view illustrating a conventional NAND type EEPROM;

[0019] Fig.2 (a) is a cross-sectional schematic diagram showing a portion of an EEPROM according to the first preferred embodiment of this invention;

[0020] Fig.2 (b) is an enlarged top view of the memory layout EEPROM of Fig.2 (a);

[0021] Fig.2 (c) is a cross-sectional view along line AA" of Fig.2 (b);

[0022] Fig.3 (a) is a cross-sectional schematic diagram showing an EEPROM according to the second preferred embodiment of the present invention;

[0023] Fig.3 (b) is a corresponding equivalent circuit of Fig.3 (a);

[0024] Fig.4 (a) is a cross-sectional schematic diagram illustrating a selected memory cell among a NAND cell block ac-

cording to this invention;

[0025] Fig.4 (b) is a table listing, by way of example, all operation parameters when operating the selected memory cell in Fig.4 (a);

[0026] Fig.5 (a) to Fig.5 (c) are a segmental circuit arrangement of the BiAND-EEPROM and exemplary operation modes thereof (erase, program, and read operations, respectively) according to the first preferred embodiment of this invention;

[0027] Fig.6 depicts a portion of a low-voltage bi-directional FN write/erase EEPROM in a cross-sectional view according to the third preferred embodiment of this invention in which only two serially connected NAND memory cell blocks B_1 and B_2 are illustrated;

[0028] Fig.7 (a) and Fig.7 (b) are shown in a cross-sectional view showing a portion of an EEPROM, and a circuit arrangement of Fig.7 (a) according to the fourth preferred embodiment of this invention;

[0029] Fig.8 (a) and Fig.8 (b) is a cross-sectional schematic diagram illustrating a 2T-BiNOR EEPROM unit and exemplary operation modes thereof (erase, program, and read operations, respectively) according to the fourth preferred embodiment of this invention;

[0030] Fig.9 (a) to Fig.9 (c) are a segmental circuit arrangement of the 2T-BiNOR-EEPROM and exemplary operation modes thereof (erase, program, and read operations, respectively) according to the fourth preferred embodiment of this invention;

[0031] Fig.10 (a) and Fig.10 (b) are an EEPROM in a cross-sectional view and corresponding equivalent circuit according to the fifth preferred embodiment of the present invention;

[0032] Fig.11 (a) and Fig.11 (b) are a cross-sectional schematic diagram illustrating a BiNOR EEPROM cell and exemplary operation modes thereof (erase, program, and read operations, respectively) according to the fifth preferred embodiment of this invention;

[0033] Fig.12 (a) to Fig.12 (c) are segmental circuit arrangement of the BiNOR EEPROM and exemplary operation modes thereof (erase, program, and read operations, respectively) according to the fifth preferred embodiment of this invention;

[0034] Fig.13 and Fig.14 illustrate other embodiments according to this invention; and

[0035] Fig.15 is a schematic cross-sectional view showing a portion of an EEPROM according to the fourth preferred em-

bodiment of this invention, wherein an induced capacitor between the CNW and the DPW during read operation is also illustrated with dash line.

DETAILED DESCRIPTION

[0036] Referring to Fig.2 (a), a portion of an EEPROM 100 is shown in a cross-sectional view according to the first preferred embodiment of this invention in which only two series connected NAND memory cell blocks B_1 and B_2 are illustrated for the sake of simplicity. As shown in Fig.2 (a), the EEPROM 100, which is based on a novel low-voltage bi-directional FN write/erase NAND type flash memory array architecture, comprises a deep P-well (hereinafter referred to as "DPW"), a cell N-well (hereinafter referred to as "CNW"), a plurality of columns of shallow P-wells (hereinafter referred to as "SPW"). Each of the plural columns of shallow P-wells, which serve as a buried local bit line during operations, is isolated from each other with shallow trench isolation (STI) regions, which are not explicitly denoted in Fig.2 (a). To isolate the shallow P-wells from each other, the thickness of the STI layer is greater than the well depth of the shallow P-wells. It is understood that only one of columns of parallel shallow P-wells is illustrated, that is, SPW_1, on which a plurality of NAND

cell blocks series connected in one column are formed, as specifically indicated in Fig.2 (a). A local bit line (hereinafter referred to as "LBL") overlies the column of NAND cell blocks. It is understood that between the B1 and B2 cell blocks, it is also possible to insert (n-2) additional memory cell blocks, where in a practical case, by way of example, n = 16.

[0037] Still referring to Fig.2 (a), each of the NAND memory cell blocks B_1 and B_2 comprises a plurality of floating gate memory cells ($M_0 \sim M_{15}$) connected in series manner. That is to say, according to the first preferred embodiment of the present invention, there are sixteen memory transistors or memory cells ($M_0 \sim M_{15}$) for each of the NAND memory cell blocks B_1 and B_2. Each of the memory cells ($M_0 \sim M_{15}$) has a stacked gate structure, i.e., upper word lines ($WL_0 \sim WL_{15}$) and floating gates. Since this invention does not specifically emphasize the structure of the memory cell units, detailed discussion on it will therefore be omitted. A source line selection transistor (SGS1) is disposed at one end of the NAND cell block B_1. The SGS1 has one terminal electrically connected to the source of the NMOS memory transistor M_{15} of the NAND cell block B_1 and another terminal electrically connected to a source line (SL)

for controlling read signals. At the other end of the NAND cell block B_1, a contact plug 102 is electrically connected with a drain 106 of the NMOS memory transistor M_0 of the NAND cell block B_1. As specifically indicated in the circle region of Fig.2 (a), the contact plug 102 penetrates a junction of the drain 106 and the underlying buried bit line SPW_1, thereby short-circuiting the drain 106 and the subjacent buried bit line SPW_1. The contact plug 102 is electrically connected to an overlying local bit line (LBL). Via a contact plug 202, LBL is electrically connected to one terminal of a main bit line selection transistor (SGB_M), which serves as a switch for controlling signals transferred from a main bit line (MBL) to the LBL. Likewise, a source line selection transistor (SGS2) is disposed at one end of the NAND cell block B_2. The SGS2 has one terminal electrically connected to the source of the NMOS memory transistor M_0 of the NAND cell block B_2 and another terminal electrically connected to the source line (SL). At the other end of the NAND cell block B_2, a contact plug 104 is electrically connected with a drain 108 of the NMOS memory transistor M_{15} of the NAND cell block B_2. The contact plug 104 penetrates a junction of the drain 108 and the underlying buried bit line SPW_1, thereby short-circuiting

the drain 108 of the memory transistor M_{15} and the subjacent buried bit line SPW_1.

[0038] Please refer to Fig.2 (b) and Fig.2 (c), where Fig.2 (b) is an enlarged top view of the memory layout EEPROM 100 of Fig.2 (a) and Fig.2 (c) is a cross-sectional view along line AA" of Fig.2 (b). As mentioned, the EEPROM 100 of the present invention comprises a plurality of columns of serially connected NAND cell blocks (C_1, C_2, C_3) and each column of cell blocks is formed on an associated SPW (SPW_1, SPW_2, SPW_3) which is isolated with STI regions. As most clearly shown in Fig.2 (c), each of the memory cells of one NAND cell block has a stacked gate structure, i.e., upper word lines (WL_n) and floating gates (F_1, F_2, F_3). According to one embodiment of this invention, the DPW is formed over an N-type semiconductor substrate.

[0039] While the above-described BiAND EEPROM memory structure according to the first preferred embodiments of the present invention has many advantages such as, among other things, low-voltage operations, high-density packing, and over-erase free, it is not perfect. For example, when implementing a page mode read operation on a 4k bit lines array, each bit line may conduct a 5μA current, and that makes a Total Required Current to 4kX5.

A=0mA. Such large read current bounce during the read operation may lead to a fluctuating read voltage or even power crash in a worse case. To overcome such potential problems during read operations, other preferred Bi-directional FN write/erase flash memory structures are proposed in this application with reference to Fig.3 to Fig.15.

[0040] Referring to Fig.3 (a) and Fig.3 (b), an EEPROM 300 in a cross-sectional view and corresponding equivalent circuit according to the second preferred embodiment of the present invention are illustrated. As shown in Fig.3 (a), the EEPROM 300, which is also based on a novel low-voltage bi-directional FN write/erase NAND (BiAND) type flash memory array architecture, comprises a DPW formed on an N-substrate, a CNW formed on the DPW, columns of isolated SPW formed within the CNW, a NAND memory cell block B formed on the SPW, and a local bit line LBL overlying the NAND memory cell block B. The NAND memory cell block B comprises a plurality of serially connected floating gate memory cells ($M_0 \sim M_7$). That is to say, according to the second preferred embodiment of the present invention, there are eight memory transistors or memory cells ($M_0 \sim M_7$) for the NAND memory cell block B.

Each of the memory cells (M_0~M_7) has a stacked gate structure, i.e., upper word lines (WL_0~WL_7) and floating gates. A source line selection transistor (SGS) is disposed at one end of the NAND cell block B. The SGS has a stacked gate structure similar to the memory cells, but the control gate and the floating gate of the SGS are electrically connected. The SGS has one terminal electrically connected to the source of the NMOS memory transistor M_7 of the NAND cell block B and another terminal electrically connected to a source line (SL) for controlling read signals. As specifically indicated with dash line, it is one of the main features of the present invention that the source line (SL) is electrically coupled to the deep P well (DPW) through the interconnection and a conductive pick up device (not shown) in accordance with one preferred embodiment of the present invention. When a read voltage, say 1.5V, is applied on the source line, a induced capacitor $C_{CNW/DPW}$ is created at the junction between the CNW and DPW, thereby stabilizing source line voltage.

[0041] At the other end of the NAND cell block B, a contact plug 302 is electrically connected with a drain of the NMOS memory transistor M_0 of the NAND cell block B. The contact plug 302 penetrates a junction of the drain and the

underlying SPW, thereby short-circuiting the drain of the memory cell M_0 and the subjacent SPW. The contact plug 302 is electrically connected to the overlying LBL. Via a contact plug 202, LBL is electrically connected to one terminal of a main bit line selection transistor (SGB_M), which serves as a switch for controlling signals transferred from a main bit line (MBL) to the LBL.

[0042] As shown in Fig.3 (b), the control gate of the SGS is electrically connected to the floating gate thereof. The SGB_M controls main bit line (MBL) signals and the SGS controls source line (SL) signals. With such configuration, the EEP-ROM 300 is capable of implementing unique low-voltage FN write/erase operations by virtue of the use of buried local bit lines (isolated SPW).

[0043] Referring to Fig.4 (a) and Fig.4 (b), where Fig.4 (a) is a cross-sectional schematic diagram illustrating a selected memory cell among a NAND cell block according to this invention and Fig.4 (b) is a table listing, by way of example, all operation parameters when operating the selected memory cell in Fig.4 (a). As mentioned, according to the present invention, the NAND memory cells are formed on an isolated SPW, which serves as a buried bit line. The LBL is electrically connected to the SPW through a contact plug

that penetrates into the substrate. Such memory structure, which is named as BiAND-EEPROM by the inventors, is capable of implementing desirable low-voltage FN tunneling write/erase operations. As shown in Fig.4 (a), in operation, a word line voltage V_{WL} is applied to the control gate 401 of the memory cell 400, a bit line voltage V_{BL} is applied to the drain 403, a source line voltage V_{SL} is applied to source 404, and a well voltage V_{DPW} is applied to DPW. Since the SPW and the drain 403 are short-circuited together, the voltage of the SPW and the voltage of the drain 403 are the same. The floating gate 402 is floating. As shown in Fig.4 (b), during an erase operation, V_{BL} is floating, $V_{WL}=10V$, $V_{SL}=-8V$, $V_{DPW}=-8V$. Under this condition, electrons are injected into and trapped in the floating gate 402 by FN tunneling through an oxide layer between the floating gate 402 and the SPW, thereby adjusting the memory cell 400 to a higher threshold voltage (higher V_{TH}) state, for example, in a range like $1.5V<V_{TH}<3.5V$. When implementing a write or program operation, $V_{BL}=5V$, $V_{WL}=-10V$, V_{SL} is floating, $V_{DPW}=0V$. Under this condition, trapped electrons in the floating gate 402 are repelled out by FN tunneling, thereby adjusting the memory cell 400 to a lower threshold voltage (lower V_{TH}) state,

for example, in a range like $V_{TH} < -1V$. When implementing a read operation, $V_{BL} = 0V$, $V_{WL} = 0V$, $V_{SL} = 1.5V$, $V_{DPW} = 0V$.

[0044] Referring to Fig.5 (a) to Fig.5 (c), a segmental circuit arrangement of the BiAND-EEPROM and exemplary operation modes thereof (erase, program, and read operations, respectively) are shown according to the first preferred embodiment of this invention. As shown in Fig.5 (a), during an erase operation, all of the word lines $WL_0 \sim WL_7$ are applied with a word line voltage of 10V, and $V_{PDW} = -8V$. All of the bit lines (only BL_1 and BL_2 are shown) are floating. Source lines (SL) are applied with a source line voltage of 8V. A gate voltage of 6V is applied to the control gate of the source line selection transistor SGS. Under this condition, electrons are injected into the floating gates of all of the flash memory cells through a so-called FN tunneling mechanism so as to adjust the threshold voltage (V_{TH}) of each of the memory cells to a relatively high V_{TH} state, preferably, in a range of $1.5V < V_{TH} < 3.5V$.

[0045] As shown in Fig.5 (b), during a data program or data write operation, a word line voltage of 10V is applied to the control gate of a selected word line WL_3, by way of example. A word line voltage of 0V is applied to the non-selected word lines, i.e., $WL_0 \sim WL_2$ and $WL_4 \sim WL_7$ within the

NAND cell block, and V_{PDW}=0V. A bit line voltage of 5V is applied to a selected bit line BL_1. Non-selected bit lines (only one non-selected bit line BL_2 is shown) are grounded. The source line (SL) is kept in a floating status. A gate voltage of 7V is applied to the control gate of the bit line selection transistor SGB. A gate voltage of 0V is applied to the control gate of the source line selection transistor SGS. Under this condition, electrons are repelled out of the floating gate of the selected flash memory cell through the FN tunneling mechanism so as to adjust the threshold voltage (V_{TH}) of each of the memory cells to a relatively low V_{TH} state, preferably, V_{TH}<-1V.

[0046] As shown in Fig.5 (c), during a data read operation, a word line voltage of 0V is applied to the control gate of a selected word line WL_3, by way of example. A word line voltage of 5V is applied to those non-selected word lines, i.e., WL_0~WL_2 and WL_4~WL_7 within the NAND cell block so as to conduct channels thereof. A source line voltage of 1.5V is applied to the source lines (SL). A bit line voltage of 0V is applied to a selected bit line BL_2. A bit line voltage of 1.5V is applied to those non-selected bit lines (only one non-selected bit line (BL_1) is shown). A gate voltage of 5V is applied to the control gate of the bit line selection

transistor SGB. A gate voltage of 5V is applied to the control gate of the source line selection transistor SGS. As aforementioned, since the source line (SL) is electrically coupled to the cell N well (CNW), an induced capacitor $C_{CNW/DPW}$ is generated at the CNW(1.5V)/DPW(ground) junction for stabilizing source line voltage.

[0047] Referring to Fig.6, a portion of a low-voltage bi-directional FN write/erase EEPROM 600 is shown in a cross-sectional view according to the third preferred embodiment of this invention in which only two serially connected NAND memory cell blocks B_1 and B_2 are illustrated for the sake of simplicity. As shown in Fig.6, the EEPROM 600 comprises a DPW, a CNW, a plurality of columns of SPWs. Each of the plural columns of SPWs, which serve as a buried local bit line during operations, is isolated from each other with STI regions. The thickness of the STI layer is greater than the well depth of the shallow P-wells. A plurality of NAND cell blocks serially connected in one column are provided. A LBL overlies the column of NAND cell blocks. Each NAND memory cell block B_1 and B_2 comprises a plurality of floating gate memory cells $(M_0{\sim}M_7)$ connected in series manner. Likewise, each of the memory cells $(M_0{\sim}M_7)$ has a stacked gate structure, i.e., upper

word lines ($WL_0 \sim WL_7$) and floating gates. A source line selection transistor (SGS1) is disposed at one end of the NAND cell block B_1. The SGS1 has one terminal electrically connected to the source of the NMOS memory transistor M_7 of the NAND cell block B_1 and another terminal electrically connected to a source line (SL) for controlling read signals. The source line is an N^+ deep doping region (N^+ SL) and is contiguous with the underlying CNW, thereby dividing the column of SPW into sub-wells (or sub-buried local bit lines): SPW_a and SPW_b corresponding to the NAND cell block B_1 and NAND cell block B_2 respectively. At the other end of the NAND cell block B_1, a contact plug is electrically connected with a drain of the NMOS memory transistor M_0 of the NAND cell block B_1. The contact plug penetrates a junction of the drain and the underlying sub-local buried bit line SPW_a, thereby short-circuiting the drain and the subjacent buried bit line SPW_a. The contact plug electrically connected to an overlying local bit line (LBL).

[0048] Referring to Fig.7 (a) and Fig.7 (b), a cross-sectional view a portion of an EEPROM 700 and a circuit arrangement of Fig.7 (a) are respectively shown according to the fourth preferred embodiment of this invention. As shown in Fig.7

(a), the EEPROM 700, which is based on a novel low-voltage bi-directional FN write/erase two-transistor NOR (2T-BiNOR) type flash memory array architecture, comprises a DPW, a CNW, a plurality of columns of shallow P-wells (SPW), a plurality of 2T memory units arranged in series on the SPW, and an LBL overlying the column of 2T memory units. Each of the plural columns of SPWs, which serve as a buried local bit line during operations, is isolated from each other with the STI regions. The thickness of the STI layer is greater than the well depth of the shallow P-wells. Each 2T memory unit comprises a memory transistor M (only $M_0 \sim M_3$ are shown) and a selection transistor SG (only $SG_0 \sim SG_3$ are shown). In this embodiment, the memory transistor M and the selection transistor SG have a similar stacked gate structure including a word line and a floating gate. It is noted that the word line and floating gate of the selection transistor sustain same voltage level during operation by electrically connecting the word line with the floating gate. The source of the memory transistor M is electrically connected to one terminal of the selection transistor SG. The drain of the memory transistor M is penetrated by a contact plug, as specifically indicated in this figure, which extends downward to

the SPW, thereby short-circuiting the drain of the memory transistor M and the SPW. The source of the selection transistor SG is preferably an N^+ deep doping region or deep source line (DSL), which is contiguous with the sub-jacent CNW. Each isolated SPW is further divided into separate sub-SPW segments by the DSL. As shown in Fig.7 (b), a main bit line selection transistor SGB_M is disposed between the main bit line and the local bit line on a P-well (PW) and is used to control signals from the main bit line to the local bit line. The selection transistor SG of the memory unit is used to control signals from the source lines (DSL). With such configuration, the EEPROM 700 of this invention is capable of implementing unique low-voltage and random access FN write/erase operations.

[0049] Referring to Fig.8 (a) and Fig.8 (b), a cross-sectional schematic diagram illustrating a 2T-BiNOR EEPROM unit 800 and exemplary operation modes thereof (erase, pro-gram, and read operations, respectively) are shown according to the fourth preferred embodiment of this inven-tion. As mentioned, the 2T-NOR EEPROM unit 800 is fab-ricated on an isolated column of SPW that serves as a buried bit line. The LBL is electrically connected to the SPW through a contact plug that penetrates the junction

between the drain of the memory transistor M and the SPW. As shown in Fig.8 (a), in operation, a word line voltage V_{WL} is applied to the control gate 801 of the memory transistor M, a bit line voltage V_{BL} is applied to the N+ drain 803. Since the SPW and the drain 803 are short-circuited together by using a plug 805, the voltage of the SPW and the voltage of the drain 803 are the same. The N^+ source 804 of the memory transistor M is serially connected to the selection transistor SG. The floating gate 802 of the memory transistor M is kept in a floating status. The control gate and floating gate of the selection transistor SG sustain same voltage level during operation by electrically connecting the word line with the floating gate. A gate voltage V_{SG} is applied to the control gate of the selection transistor SG. A source line voltage V_{SL} is applied to the N+ source 806 of the selection transistor SG, which is an N^+ deep source line (DSL) and is contiguous with the subjacent cell N-well. A well voltage V_{DPW} is applied to the DPW.

[0050] As shown in Fig.8 (b), during an erase operation, V_{BL} is floating, $V_{WL}=10V$, $V_{SL}=-8V$, $V_{SG}=-6V$, $V_{DPW}=-8V$. Under this condition, electrons are injected into and trapped in the floating gate 802 by FN tunneling through an oxide layer between the floating gate 802 and the SPW, thereby

adjusting the memory cell 800 to a higher threshold voltage (higher V_{TH}) state, for example, in a range like $1.5V < V_{TH} < 3.5V$. When implementing a program operation, $V_{BL} = 5V$, $V_{WL} = -10V$, V_{SL} is floating, $V_{DPW} = 0V$, $V_{SG} = 0V$. Under this condition, trapped electrons in the floating gate 802 are repelled out by FN tunneling, thereby adjusting the memory cell 800 to a lower threshold voltage (lower V_{TH}) state, for example, in a range like $V_{TH} < -1V$. When implementing a read operation, $V_{BL} = 0V$, $V_{WL} = 0V$, $V_{SL} = 1.5V$, $V_{DPW} = 0V$, and $V_{SG} = 5V$.

[0051] Referring to Fig.9 (a) to Fig.9 (c), a segmental circuit arrangement of the 2T-BiNOR-EEPROM and exemplary operation modes thereof (erase, program, and read operations, respectively) are shown according to the fourth preferred embodiment of this invention. As shown in Fig.9 (a), during an erase operation, all of the word lines (only $WL_0 \sim WL_3$ are shown) are applied with a word line voltage of 10V, and $V_{PDW} = -8V$. All of the bit lines (only BL_1 and BL_2 are shown) are floating. Source lines (SL) are applied with a source line voltage of 8V. A gate voltage of 6V is applied to the control gate of the source line selection transistor SG (only $SG_0 \sim SG_3$ are shown). A gate voltage of 8V is applied to the control gate of the bit line selection transistor

SGB. Under this condition, electrons are injected into the floating gates of all of the memory transistors through the FN tunneling mechanism so as to adjust the threshold voltage (V_{TH}) of each of the memory cells to a relatively high V_{TH} state, preferably, in a range of $1.5V<V_{TH}<3.5V$.

[0052] As shown in Fig.9 (b), during a data program operation, a word line voltage of 10V is applied to the control gate of a selected word line WL_1, by way of example. A word line voltage of 0V is applied to the non-selected word lines, i.e., WL_0, WL_2 and WL_3. V_{PDW}=0V. A bit line voltage of 5V is applied to a selected bit line BL_1. Non-selected bit lines (only one non-selected bit line BL_2 is shown) are grounded. The source line (SL) is kept in a floating status. A gate voltage of 7V is applied to the control gate of the bit line selection transistor SGB. A gate voltage of 0V is applied to the control gate of the source line selection transistor SG. Under this condition, electrons are repelled out of the floating gate of the selected memory transistor through the FN tunneling mechanism so as to adjust the threshold voltage (V_{TH}) of each of the memory cells to a relatively low V_{TH} state, preferably, $V_{TH}<-1V$.

[0053] As shown in Fig.9 (c), during a data read operation, a word line voltage of 0V is applied to the control gate of a

selected word line WL_1, by way of example. A gate voltage of 5V is applied to the control gate of a selection transistor connected to the selected memory transistor. A word line voltage of 0V is applied to those non-selected word lines, i.e., WL_0, WL_2, and WL_3 so as to conduct channels thereof. A gate voltage of 0V is applied to those non-selected selection transistors SG_0, SG_2, SG_3. A source line voltage (V_{SL}) of 1.5V is applied to the source lines (SL). The DPW is connected to ground $(V_{DPW}=0V)$. A bit line voltage of 0V is applied to a selected bit line BL_2. A bit line voltage of 1.5V is applied to those non-selected bit lines (only one non-selected bit line (BL_1) is shown). A gate voltage of 5V is applied to the control gate of the bit line selection transistor SGB. It is one of the main features of the present invention that the source line is electrically coupled to the cell N well to avoid aforementioned large read current bounce or potential power crash. This is because, under the above-described read voltage conditions, a large capacitance is created at the junction between the cell N well (CNW) and the underlying deep P well (DPW). As specifically indicated in Fig.9(c) and Fig.15, the induced capacitor "$C_{CNW/DPW}$" formed between the CNW and the DPW due to the formation of the depletion region

therebetween is charged up during the read operation and therefore helps to stabilize source line voltage.

[0054] Referring to Fig.10 (a) and Fig.10 (b), an EEPROM 1000 in a cross-sectional view and corresponding equivalent circuit according to the fifth preferred embodiment of the present invention are illustrated. Compared to the fourth embodiment of this invention, the fifth preferred embodiment of this invention has no selection transistors (SG) formed on the SPW in the memory array. Consequently, it is particularly suited for high-density data flash memory. As shown in Fig.10 (a), EEPROM 1000, which is based on a novel low-voltage bi-directional FN write/erase NOR type (BiNOR) flash memory array architecture, comprises a DPW formed on an N-substrate, a CNW formed on the DPW, columns of isolated SPW formed within the CNW, a plurality of memory cells $(M_0 \sim M_7)$ formed on the SPW, and a local bit line LBL overlying the memory cells $(M_0 \sim M_7)$. Each memory cell $(M_0 \sim M_7)$ has a stacked gate structure, i.e., upper word lines $(WL_0 \sim WL_7)$ and floating gates. The source of each of the memory cells $(M_0 \sim M_7)$ is an N^+ deep doping region (DSL) and is contiguous with the underlying CNW, thereby dividing the column of SPW into sub-wells. The drain of each of the memory cells $(M_0 \sim M_7)$ is pene-

trated by a contact plug, which extends downward to the SPW, thereby short-circuiting the drain and the SPW. As shown in Fig.10 (b), a main bit line selection transistor SGBis disposed between the main bit line and the local bit line and is used to control signals from the main bit line to the local bit line. With such configuration, the EEPROM 1000 of this invention is capable of implementing unique low-voltage and random access FN write/erase operations.

[0055] Referring to Fig.11 (a) to Fig.11 (c), a cross-sectional schematic diagram illustrating a BiNOR EEPROM cell 1100 and exemplary operation modes thereof (erase, program, and read operations, respectively) are shown according to the fifth preferred embodiment of this invention. As mentioned, the BiNOR EEPROM unit 1100 is fabricated on an isolated column of SPW that serves as a buried bit line. The LBL is electrically connected to the SPW through a contact plug that penetrates the junction between the drain of the memory cell and the subjacent SPW. As shown in Fig.11 (a), in operation, a word line voltage V_{WL} is applied to the control gate 1101 of the memory transistor 1100, a bit line voltage V_{BL} is applied to the N+ drain 1103. Since the SPW and the drain 1103 are short-circuited to-

gether by using a plug 1105, the voltage of the SPW and the voltage of the drain 1103 are the same. A source voltage V_{SL} is applied to the N^+ source 1104 of the memory transistor 1100. The N^+ source 1104 is an N^+ deep doping region and is contiguous with the subjacent cell N-well. The floating gate 1102 of the memory transistor 1100 is kept in a floating status. A well voltage V_{DPW} is applied to the deep P-well.

[0056] As shown in Fig.11 (b), during an erase operation, V_{BL} is floating, $V_{WL}=10V$, $V_{SL}=-8V$, $V_{DPW}=-8V$. Under this condition, electrons are injected into and trapped in the floating gate 1102 by FN tunneling through an oxide layer between the floating gate 1102 and the SPW, thereby adjusting the memory cell 1100 to a higher threshold voltage (higher V_{TH}) state, for example, $V_{TH} > 6V$. When implementing a program operation, $V_{BL}=5V$, $V_{WL}=-10V$, V_{SL} is floating, $V_{DPW}=0V$. Under this condition, trapped electrons in the floating gate 1102 are repelled out by FN tunneling, thereby adjusting the memory cell 1100 to a lower threshold voltage (lower V_{TH}) state, for example, in a range like $1V<V_{TH}<2V$. When implementing a read operation, $V_{BL}=0V$, $V_{WL}=4V$, $V_{SL}=1.5V$, $V_{DPW}=0V$.

[0057] Referring to Fig.12 (a) to Fig.12 (c), a segmental circuit ar-

rangement of theBiNOR EEPROM and exemplary operation modes thereof (erase, program, and read operations, respectively) are shown according to the fifth preferred embodiment of this invention. As shown in Fig.12 (a), during an erase operation, all of the word lines (WL_0~WL_7) are applied with a word line voltage of 10V, and V_{PDW}=-8V. All of the bit lines (only BL_1 and BL_2 are shown) are floating. Source lines (SL) are applied with a source line voltage of -8V. A gate voltage of 8V is applied to the control gate of the bit line selection transistor SGB. Under this condition, electrons are injected into the floating gates of all of the memory transistors through the FN tunneling mechanism so as to adjust the threshold voltage (V_{TH}) of each of the memory cells to a relatively high V_{TH} state, preferably, V_{TH} > 6V.

[0058] As shown in Fig.12 (b), during a data program operation, a word line voltage of 10V is applied to the control gate of a selected word line WL_3, by way of example. A word line voltage of 0V is applied to the non-selected word lines, i.e., WL_0~WL_2 and WL_4~WL_7. V_{PDW}=0V. A bit line voltage of 5V is applied to a selected bit line BL_1. Non-selected bit lines (only one non-selected bit line BL_2 is shown) are grounded. The source line (SL) is kept in a floating status.

A gate voltage of 7V is applied to the control gate of the bit line selection transistor SGB. Under this condition, electrons are repelled out of the floating gate of the selected memory transistor through the FN tunneling mechanism so as to adjust the threshold voltage (V_{TH}) of each of the memory cells to a relatively low V_{TH} state, preferably, $1V < V_{TH} < 2V$.

[0059] As shown in Fig.12 (c), during a data read operation, a word line voltage of 4V is applied to the control gate of a selected word line WL_3, by way of example. A word line voltage of 0V is applied to those non-selected word lines $WL_0 \sim WL_2$ and $WL_4 \sim WL_7$. A source line voltage of 1.5V is applied to the source lines (SL) that is electrically coupled to the CNW. The DPW is connected to ground ($V_{DPW} = 0V$). A bit line voltage of 0V is applied to a selected bit line BL_2. A bit line voltage of 1.5V is applied to those non-selected bit lines (only one non-selected bit line (BL_1) is shown). A gate voltage of 7V is applied to the control gate of the bit line selection transistor SGB. Likewise, a large capacitance is created at the junction between the cell N well (CNW) and the underlying deep P well (DPW) to avoid large read current bounce or potential power crash.

[0060] Referring to Fig.13 and Fig.14, other embodiments ac-

cording to this invention are shown. In Fig.13, a one-MBL-to-one-LBL layout is illustrated. Bit line signals from the MBL1 to the LBL1 are controlled by a SGB$_{M1}$. Bit line signals from the MBL2 to the LBL2 are controlled by a SGB$_{M2}$. In Fig.14, a one-MBL-to-two-LBL layout is illustrated.

[0061] Those skilled in the art will readily observe that numerous modification and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.